WHAT IS CLAIMED IS:

1. A liquid crystal display device comprising:

a display part divided into blocks;

a gate driver which sequentially drives scan lines arranged in the display part one by one; and

a data driver which supplies, via common signal lines, display signals to pixels connected to one of the scan lines driven by the gate driver and located in one of the blocks which are sequentially selected in accordance with a block control signal.

2. The liquid crystal display device as claimed in claim 1, further comprising a block control signal generating part which generates the block control signal.

3. The liquid crystal display device as claimed in claim 1, further comprising an electronic circuit which is provided to a panel substrate on which the display part is formed and which generates the block control signal.

4. The liquid crystal display device as claimed in claim 1, further comprising an electronic circuit which is provided outside a panel substrate on which the display part is formed and which generates the block control signal.

5. The liquid crystal display device as claimed in claim 1, further comprising analog switches located in the blocks and provided between the common signal lines and the pixels, the analog switches located in said one of the blocks selected by the block control signal being simultaneously activated.

6. The liquid crystal display device as claimed in claim 5, wherein:

each of the analog switches comprises a pair of an n-channel field effect transistor and a p-channel field effect transistor and is connected to a corresponding one of the common signal lines via which the block control signal having different polarities are supplied; and

the display signals are applied to the pixels from the common signal lines via one of each of pairs of analog switches selected by block control signals separately supplied.

7. The liquid crystal display device as

claimed in claim 5, wherein:

said analog switches re formed by either n-channel or p-channel TFTs, connected to one of the common signal lines, and controlled by the block control signals; and

the display signals are applied to the pixels from the common signal lines via one of the analog switches selected by a corresponding one of the block control signals.

8. The liquid crystal display device as claimed in claim 1, wherein said data driver comprises a display signal generating parts which generates the display signals from a digital signal applied thereto and applies the display signals to said one of the blocks selected in accordance with the block control signal.

9. The liquid crystal display device as claimed in claim 1, wherein said display signal generating part comprises at least one driver IC mounted by a TAB, TCP or COG, output terminals of the at least one driver IC being connected to the common signal lines.

10. The liquid crystal display device as claimed in claim 9, wherein the output terminals of the at least one driver IC are connected to output

terminals an IC chip, output terminals of the gate driver, output terminals of the data driver and control terminals of the analog switches.

11. The liquid crystal display device as claimed in claim 1, wherein a number of the common signal lines is larger than a number of blocks.

12. The liquid crystal display device as claimed in claim 1, wherein a block control period during which one of the blocks is activated is longer than a time constant of signal lines which are provided in the display part and coupled to the common signal lines.

13. The liquid crystal display device as claimed in claim 1, wherein a blanking period during which the clock control signals are not supplied to any of the blocks is longer than a block control period during which one of the blocks is activated or a sum of a rising time and a falling time of a gate scan signal which sequentially drives the scan lines.

14. The liquid crystal display device as

claimed in claim 1, wherein at least one of the gate driver and the data driver includes a plurality of chips.

15. The liquid crystal display device as claimed in claim 5, wherein the analog switches in one of the blocks are simultaneously turned on in response to the block control signal.

16. The liquid crystal display device as claimed in claim 1, wherein the display part comprises a number of pixels which is an integer multiple of a number of bits of one block.

17. The liquid crystal display device as claimed in claim 16, wherein each of the blocks comprises a number of bits equal to an integer multiple of any of 200, 240, 256, 300 and 384.

18. The liquid crystal display device as claimed in claim 1, wherein the display part and the gate driver and the analog switches are formed on an identical substrate and the data driver is formed by an TAB-IC provided outside the substrate.

19. The liquid crystal display device as claimed in claim 1, wherein segmented areas are defined so as to correspond to the blocks, each of the segmented areas having a respective width of the block control lines.

20. The liquid crystal display device as claimed in claim 19, wherein an expression described below is satisfied:

$$w = (Wo - (n - 1)S)/n$$

where Wo denotes a width of each of the segmented areas, w denotes a width of the block control lines, n denotes a number of block control lines, and S denotes an interval between adjacent ones of the block control lines.

21. The liquid crystal display device as claimed in claim 19, wherein the width of the block control lines in each of the segmented areas is selected so that the block control lines in each of the segmented areas have an approximately constant resistance value measured from start points of the block control lines to end points thereof.

22. The liquid crystal display device as claimed in claim 19, wherein the block control lines have a multi-layer structure having an upper block control line and a lower block control line, the

upper and lower block control lines being electrically connected via a through hole formed in an insulating layer sandwiched between the upper and lower control lines.

23. The liquid crystal display device as claimed in claim 19, further comprising a signal line connecting the switch elements arranged in an identical one of the blocks, a corresponding one of the block control lines being connected to a central portion of the signal line connecting the switch elements.

24. The liquid crystal display device as claimed in claim 1, wherein each of the blocks having a respective resistivity of the block control lines so that differences between resistance values of the block control lines measured from start points of the block control lines to end points thereof can be reduced.

25. The liquid crystal display device as claimed in claim 24, wherein each of the blocks has a respective layer structure dependent on the corresponding resistivity.

26. A liquid crystal display device comprising:

a display part having pixels arranged in a matrix formation;

signal lines and scan lines connected to the pixels;

a data driver which supplies display signals to the signal lines; and

a reset circuit which resets the potentials of the signal lines to a predetermined potential with a given period.

27. The liquid crystal display device as claimed in claim 26, wherein the reset circuit is connected to the signal lines.

28. The liquid crystal display device as claimed in claim 26, wherein the reset circuit is connected to an output part of the data driver.

29. The liquid crystal display device as claimed in claim 26, wherein the reset circuit comprises a first reset circuit connected to the signal lines, and a second reset circuit connected to an output part of the driver.

30. The liquid crystal display device as claimed in claim 26, wherein the reset circuit receives a reset signal externally applied thereto during a blanking period included in a horizontal period and resets the potentials of the signal lines to the predetermined potential during the blanking period.

31. The liquid crystal display device as claimed in claim 26, wherein a polarity of the predetermined potential is inverted in synchronism with the polarity of the display signals.

32. A liquid crystal display device comprising:

a display part having pixels arranged in a matrix formation;

signal lines and scan lines connected to the pixels;

analog switches respectively connected to the signal lines;

a data driver which is connected to the analog switches via common signal lines and supplies display signals to the signal lines via the analog switches; and

a reset circuit which resets the potentials of the signal lines and/or the common signal lines to a predetermined potential with a given period.

33. The liquid crystal display device as claimed in claim 32, wherein the reset circuit is connected to the signal lines.

34. The liquid crystal display device as claimed in claim 32, wherein the reset circuit is connected to an output part of the driver.

35. The liquid crystal display device as claimed in claim 32, wherein the reset circuit comprises a first reset circuit connected to the signal lines, and a second reset circuit connected to an output part of the driver.

36. The liquid crystal display device as claimed in claim 32, wherein the reset circuit is connected to the common signal lines.

37. The liquid crystal display device as claimed in claim 32, wherein the reset circuit comprises a first reset circuit connected to the signal lines, and a second reset circuit connected to either an output part of the driver or the common signal lines.

38. The liquid crystal display device as claimed in claim 32, wherein the reset circuit receives a reset signal externally applied thereto during a blanking period included in a horizontal period and resets the potentials of the signal lines to the predetermined potential during the blanking period.

39. The liquid crystal display device as claimed in claim 32, wherein a polarity of the predetermined potential is inverted in synchronism with the polarity of the display signals.

40. A liquid crystal display device comprising:

a display part which has pixels arranged in a matrix formation and is divided into blocks;

signal lines and scan lines connected to the pixels;

analog switches respectively connected to the signal lines and provided in the blocks;

a data driver which is connected to the analog switches via common signal lines and supplies display signals to the signal lines via the analog switches provided in one of the blocks which are sequentially selected in accordance with a block control signal; and

a reset circuit which resets the potentials of the signal lines to a predetermined potential with a given period.

41. The liquid crystal display device as claimed in claim 40, wherein the reset circuit receives a reset signal externally applied thereto during a blanking period included in a horizontal scan period and resets the potentials of the signal lines to the predetermined potential during the blanking period.

42. A data driver comprising:

an internal IC circuit which generates display signals formed on a substrate;

operational amplifiers connected to the internal IC circuit; and

a reset circuit which resets a potential of an output part to a predetermined potential, the display signals being output via the output part of the reset circuit.